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(54) FIELD EFFECT TRANSISTORS

(71) We, SONY CORPORATION, a corporation organized and existing under the laws of Japan of 7—35 Kitashinagawa-6, Shinagawa-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to field effect transistors, and more particularly to MIS field effect transistors and semiconductor devices including such transistors.

Double-diffused MIS transistors have been previously proposed, for example in "Electronics", 15 February 1971, pages 99 to 104. The double-diffused MIS transistor has a very narrow channel determined by a two-stage diffusion through a single mask opening. As the frequency response of any MIS transistor is determined primarily by channel length, the double-diffused MIS transistor has a good frequency response.

The semiconductor substrate usually has a low impurity concentration, such as 10^{14} to 10^{16} atoms/cm^{3}, so the capacitance of the P—N junction formed between the drain and the substrate is small. Accordingly, when the substrate is earthed, in order to apply earth potential to the channel region, the spreading resistance in the substrate, which is rather large, impairs the overall frequency response.

According to the present invention there is provided an MIS field effect transistor comprising:

a semiconductor body including:

first and second regions of semiconductor material of one conductivity type;

a third, cup-shaped, region of semiconductor material of opposite conductivity type, said third region enclosing said second region and forming a PN junction therewith and a further PN junction with said first region, and the edge of said third region being located at a surface of said body; and

a fourth region of semiconductor material of said opposite conductivity type and greater impurity concentration than said third region located beneath and in contact with said third region; and

first and second electrodes respectively connected to said first and second regions.

a gate electrode insulated from said surface and positioned over said edge of said third region; and

means to enable a potential to be applied to said third region through said fourth region.

The invention will now be described by way of example with reference to the accompanying drawings, in which:—

Figure 1 is a sectional view of a known MIS field effect transistor;

Figure 2 is a sectional view of an MIS field effect transistor according to the present invention;

Figures 3A to 3G show steps in manufacturing another embodiment of the present invention, comprising a semiconductor integrated circuit having an MIS field effect transistor and a conventional bipolar transistor;

Figure 4 is a sectional view of a known cascaded pair of double-diffused MIS field effect transistors; and

Figure 5 is a sectional view of a double-diffused MIS tetrode according to the present invention applied in a device similar to that of Figure 4.

For a better understanding of the present invention, a known double-diffused MIS field effect transistor will first be described with reference to Figure 1.

On a semiconductor body which forms a P-type substrate region 1 of, for example, low impurity concentration, and N-type semiconductor layer 2 of low impurity concentration is formed by epitaxial growth and a P-type channel region 3 is selectively formed in the semiconductor layer 2. An N-type source region 4 of high impurity concentration is formed in the channel region 3 by diffusion at the position in alignment with a window of a mask used for forming the

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channel region 3 in a selective diffusion process, or by means of a common window of the mask. The diffusion depth of the source region 4 is made smaller than that of the channel region 3. The channel region 3 thus becomes cup-shaped with its edge in the surface of the semiconductor body. At the same time as the source region 4 is formed by diffusion, a high impurity region 6 for drain electrode contact is formed at the central portion of an N-type drain region 5 which is adjacent to the channel region 3, the high impurity region 6 forming a part of the drain region 5. A gate insulating layer 7 is formed on the channel region 3 between the source region 4 and the drain region 5, and a gate electrode 8 is formed on the gate insulating layer 7. The source electrode 9 is formed on the source region 4 and a drain electrode 10 is formed on the region 6.

With such an MIS field effect transistor, since a length l of the channel portion of the channel region 3 beneath the gate insulating layer 7 and between the regions 4 and 5 or a length l of a portion c, where an inversion layer is formed, is determined in accordance with the difference between diffusion widths of the regions 4 and 5 in the lateral direction, the length l can be made small enough to increase the mutual conductance gm and the MIS field effect transistor can be made in an integrated circuit substrate simultaneously with other semiconductor elements, because it is formed by a so-called planar technique.

However, in the MIS field effect transistor constructed as above, in order to decrease the capacity of a P—N type junction j formed between the drain region 5 and the substrate 1, the impurity concentration of the substrate 1 is made low, for example, from 10^{14} to 10^{16} atoms/cm^3. Accordingly, if an electrode is formed on the outer side of the substrate 1 for applying earth potential to, for example, the channel region 3, the high-frequency characteristics are impaired due to large resistance resulting from the high resistivity of the substrate 1.

It may also be possible for providing such an electrde that, as shown in Figure 1 by dotted lines, a diffusion region 11 for ohmic contact, which region 11 is of the same conductivity type as the channel region 3, is formed in the semiconductor layer 2 touching one side of the channel region 3, and an electrode 12 is attached to the diffusion layer 11 in ohmic contact. In this case, however, the spreading resistance of the channel region 3 is large and the diffusion region 11 must be of substantial area.

A field effect transistor according to the present invention will now be described with reference to Figure 2, in which similar reference numerals to those of Figure 1 designate similar elements, the descriptions of which will be omitted.

The substrate 1, which has a relatively low impurity concentration of 10^{14} to 10^{16} atoms/cm^3, extends beneath at least the drain electrode 10, or beneath the high impurity concentration region 6 for the drain electrode 10. A buried layer 18, which has a relatively high impurity concentration, for example, from 10^{18} to 10^{20} atoms/cm^3, is low in resistivity and is of the same conductivity type as the channel region 3, is buried in the layer 2 and the substrate 1 under the channel region 3. The buried layer 18 contacts the bottom of the channel region 3 over as great a width as possible. A region 14 of P-type high impurity concentration is provided under the buried layer 18 and the substrate 1, and the electrode 12 is connected in ohmic contact to the outer surface of the region 14.

With the field effect transistor constructed as described above, since the buried layer 18 of high impurity concentration is provided under the channel region 3, the spreading resistance of the channel region 3 can be made low. Moreover, as the region 14 of high impurity concentration is provided with the electrode 12 for the channel region 3 on the outer surface of the region 14, there is no need to provide the diffusion region 11 shown in Figure 1, and so the size of the device can be reduced.

Further, the substrate 1, which is of low impurity concentration, contacts the drain region 5, especially the portion opposing the drain electrode 10 to which a bias voltage is applied, and the portion opposing the high impurity region 6, so that the capacity of the P—N junction j therebetween can be made small even if the spreading resistance of the channel region 3 is low. This improves the resistance to breakdown.

An embodiment comprising a semiconductor integrated circuit including an N-channel MIS field effect transistor and an NPN transistor, and the method of making it, will now be described with reference to Figures 3A to 3G.

First, as shown in Figure 3A, a semiconductor substrate or wafer, for example, a silicon substrate 15 of P-type conductivity and high impurity concentration, from 10^{18} to 10^{20} atoms/cm^3, is prepared. Then, a semiconductor layer, for example, a silicon layer 16 which has relatively low impurity concentration from 10^{14} to 10^{16} atoms/cm^3 and the same conductivity type as the substrate 15 is formed on the latter by epitaxial growth.

As shown in Figure 3B, a collector buried layer 17 of N-type conductivity and high impurity concentration is then selectively formed in the semiconductor layer 16 at the position where is opposes the collector junction of an NPN transistor which is to be formed. A buried layer 18 of P-type conduc-

tivity and high impurity concentration is formed in the layer 16 at the position opposing the channel region of an MIS field effect transistor which is to be formed, so as to reduce the resistance of the channel region, and a buried layer 19 for isolation is also formed in the layer 16 at the position where the drain region of the MIS field effect transistor must be electrically isolated from the NPN transistor. The latter buried layer 19 for isolation may appear in plan as a lattice or of annular shape.

As shown in Figure 3C, a semiconductor, for example, silicon layer 20 of N-type conductivity and relatively low impurity concentration, for example, from 10^{15} to 10^{16} atoms/cm^3 is epitaxially grown on the semiconductor layer 16. By heating during the formation of the layer 20 or by further heat treatment, the impurities in the respective buried layers 17, 18 and 19 are diffused upwardly into the semiconductor layer 20 to extend the layers 17, 18 and 19 into the layer 20. Since the diffusion coefficients of the impurities in the layers 18 and 19 are greater than that of the impurity in the layer 17, the extension lengths of the layers 18 and 19 in the semiconductor layer 20 are larger than that of the layer 17 in the layer 20. The impurity concentrations of thus formed layers 17, 18 and 19 are approximately from 10^{18} to 10^{20} atoms/cm^3.

An insulating layer 21 such as, for example, a silicon dioxide layer, which will be used as a diffusion mask, is coated on the layer 20. Windows 22, 23 and 24 are formed in the insulating layer 21 by photo engraving or etching at the positions corresponding to the buried layers 17, 18 and 19. A further window 25 is also formed in the insulating layer 21 at the position corresponding to the layer 18 with a predetermined distance from the window 22. In this case, the window 24 is formed with a lattice or annular shape to correspond to the full area of the layer 19.

Referring now to Figure 3D, through the mask, in particular through the windows 22, 23, 24 aand 25 in the insulating layer 21, a P-type impurity is diffused into the layer 20 to form a base region 26*b*, a channel region 3, an isolation region 27 and a region 28 for making an ohmic contact. The diffusion depths of the regions 3, 28 and 27 are so selected that they reach the buried layers 18 and 19, but the depth of the base region 26*b* is so selected that it does not reach the buried layer 17.

Thus, the semiconductor layer 20 is divided, by the buried layer 19 and the diffusion layer 27, into a part 20A which will form the MIS field effect transistor and a part 20B which will form the NPN transistor. In the part 20A, there are formed the channel region 3 and the drain region 5 consisting of the N-type region of the semiconductor layer 20 in which the channel region 3 is not formed. In the part 20B there are formed the base region 26*b* and a collector region 26*c* consisting of the N-type region of the semiconductor layer 20 in which the base region 26*b* is not formed.

When the respective regions 26*b*, 3, 27 and 28 are formed by diffusion, the surface of the semiconductor layer 20 exposed outside through the windows 22, 23, 24 and 25 may be oxidised to close these windows with the insulating layer 21.

Referring now to Figure 3E, the parts of the insulating layer 21 on the base region 26*b*, the drain region 5 and the channel region 3 are removed to form windows 29, 30 and 31. The windows 29 and 30 may be formed by, for example, a photoetching process, but it is required that the window 31 on the channel region 3 coincides in position with the window 23 used when the channel region 3 was formed. For this purpose, it utilised the fact that the insulating layer 21 formed in the window 23 during the diffusion process forming the channel region 3 is thinner than that at the marginal portions of the window 23. The insulating layer 21 within the window 23 is therefore removed by etching to provide the window 31 in coincidence with the window 23.

Referring to Figure 3F, through these windows 29, 30 and 31 an N-type impurity of high concentration is diffused into the regions 26*b*, 5 and 3, to form an emitter region 26*e*, a drain region 6 for the drain electrode and a source region 4. The drain region 6 is formed in the position where it does not oppose the buried layer 18. In other words, the buried layer 18 is not positioned under the region 6.

If necessary, it may be possible to remove by etching the insulating layer 21 between the source region 4 and the drain region 5 on the channel region 3 and to form the gate insulating layer 7 instead. On the gate insulating layer 7 the gate electrode 8 is formed. The source electrode 9 and the drain electrode 10 are respectively provided in ohmic contact with the source region 4 and the drain region 6 through windows formed through the insulating layer 21 on the source region 4 and the drain region 6 respectively. At the same time, a window is formed in the insulating layer 21 on the region 28, and the electrode 12 is formed in ohmic contact with the region 28 through the window. Simultaneously, windows are formed in the insulating layer 21 on the emitter region 26*e*, the base region 26*b* and the collector region 26*c*, and through thus formed windows an emitter electrode 32*e*, a base electrode 32*b* and a collector electrode 32*c* are, respectively, formed in ohmic contact with the corresponding regions. Thus, as shown

in Figure 3G, a semiconductor integrated circuit is obtained in which on the common semiconductor substrate 40 there are provided an MIS field effect transistor M_T and an NPN-type transistor Tr. The MIS field effect transistor M_T and the NPN-type transistor Tr are electrically isolated by the P—N junction *j* formed between the collector region 26*c* of N-type conductivity, the buried layer 17 of the same conductivity type and the P-type conductivity isolation regions 27, 19 and the semiconductor layer 16 of the same conductivity type.

In the foregoing embodiment, the window 31 for providing the source region 4 coincides with the window 23 used for providing the channel region 3, but in practice it is enough that the window 31 coincides with the window 23 is such a manner that the marginal portion of the inversion layer, namely the side for providing a channel *c* of the former window coincides with the corresponding marginal portion of the latter window.

With the integrated circuit formed as described above, since the buried layer I8 of high impurity concentration is provided at the bottom portion of the channel region 3 for the MIS field effect transistor M_T, the spreading resistance of the channel region 3 is low, which improves the high frequency characteristic of the transistor M_T.

The burried layer 18 is selectively formed and opposing the part of region 5 forming the region 6 for the drain electrode 10 is a substrate formed by the semiconductor layer 16 of low impurity concentration, so the capacitance between the drain and the substrate can be made small. Further, since the buried layer 18 is selectively formed, other circuit elements, for example, NPN-type transistors can be formed in the common semiconductor substrate 40.

In the foregoing embodiment, the MIS field effect transistor M_T and the bipolar transistor Tr are provided but it may be possible that, instead of or in addition to the transistor Tr, other circuit elements are formed to provide an integrated circuit.

Further, as shown in Figure 4, in which reference numerals similar to those in the foregoing figures refer to similar elements, two MIS field eect transistors MIS_1 and MIS_2 can be formed on a common semiconductor substrate 30 and when the two MIS transistors MIS_1 and MIS_2 are connected in cascade, the feedback capacity can be reduced.

Previously when two MIS transistors have been connected in cascade, the drain of one MIS transistor is connected to the source of the other MIS transistor. In other words, a so-called MIS tetrode is formed on the common semiconductor substrate 30 of P-type conductivity with the NPN-type bipolar transistor Tr and regions 31A, 31B and 31C of N-type conductivity, separately formed in the semiconductor substrate 30. One MIS field effect transistor MIS_1 is formed in the region 31A, the other MIS field effect transistor MIS_2 is formed in the region 31B, and the bipolar transistor Tr in the region 31C. A P-type channel region 3A and an N-type source region 4A are formed in the region 31A by diffusion through windows whose marginal edges on the side where channels are formed finally are common. The portion of the region 31A where the regions 3A and 4A are not formed is used as a drain region 5A. Meanwhile, in the region 31B there are formed a channel region 3B, a source region 4B and a drain region 5B by a similar method in correspondence with the regions 3A, 4A and 5A formed in the region 31A. A first gate isolating layer 7A is formed on the channel region 3A between the source region 4A and the drain region 5A and a first gate electrode 8A is formed on the first gate isolating layer 7A. Similarly, a second gate isolating layer 7B is formed on the channel region 3B between the source region 4B and the drain region 5B and a second gate electrode 8B is formed on the second gate isolating layer 7B. First and second source electrodes 9A and 9B are provided on the source regions 4A and 4B respectively in ohmic contact therewith, and first and second drain electrodes 10A and 10B are provided on the drain regions 5A and 5B respectively in ohmic contact therewith. The drain electrode I0A of the first MIS field effect transistor MIS_1 is connected to the source electrode 9B of the second MIS field effect transistor MIS_2 by means of a lead wire 3I or an interconnection formed by a conductive layer. Electrodes 12A and 12B are provided on the first and second channel regions 3A and 3B respectively in ohmic contact therewith, for applying a predetermined potential, for example, an earth potential to the latter. In the region 31C, which is taken as, for example, a collector region 26*c*, a P-type base region 26*b* is formed and an N-type emitter region 26*e* is formed in the base region 26*b*. A collector electrode 32*c*, a base electrode 32*b* and an emitter electrode 32*e* are respectively provided on the regions 26*c*, 26*b* and 26*e* in ohmic contact therewith to form the transistor Tr.

With such a construction, however, there is a drawback that the spreading resistance of the channel regions 3A and 3B of the first and second MIS field effect transistors MIS_1 and MIS_2 becomes large.

Further, in such a construction, the area of the drain region 5A of the first MIS field effect transistor MIS_1 covers the whole of the channel region 3A and is relatively large, and a P—N junction J_D formed on the outer

surface of the drain region 5A is large in area, so that its junction capacity is also large.

Figure 5 shows an embodiment in which the present invention is applied to the integrated circuit construction shown in Figure 4. In Figure 5, reference numerals similar to those in Figure 4 designate similar elements and their description will be omitted for the sake of simplicity. In Figure 5, the transistor Tr is formed in, for example, the region 31C in a similar manner to that described in connection with Figure 4 and the two MIS field effect transistors MIS_1 and MIS_2 are formed in a common region 31A' of N-type conductivity. An impurity of P-type conductivity is selectively diffused into the region 31A' to form two separate channel regions 3A and 3B of P-type conductivity and then an impurity of N-type conductivity is diffused into the two channel regions 3A and 3B respectively, through the same windows which are used when the channel regions 3A and 3B are formed to form source regions 4A and 4B. Further, a diffusion region 4B' of N-type conductivity is formed adjacent to the source region 4B of the second MIS field effect transistor MIS_2 at the position opposing the first MIS field effect transistor MIS_1 thereby to connect the second source region 4B to an island region 33 of N-type conductivity formed in the region 31A' between the two channel regions 3A and 3B. Thus, the island region 33 serves as the drain region 5A of the first MIS field effect transistor MIS_1 and the source region 4B of the second MIS field effect transistor MIS_2 is connected to the island region 33 through the region 4B', so that the drain electrode 10A which is necessary in the arrangement of Figure 4 can be dispensed with. Thus, a so-called MIS tetrode, which is constructed by cascading the first and second MIS field effect transistors MIS_1 and MIS_2, can be obtained.

In the present case the buried layer 18 of high impurity concentration and the same conductivity type as the channel regions 3A and 3B is formed in the semiconductor substrate 30 at the position corresponding to the bottoms of the two channel regions 3A and 3B and extending across both regions 3A and 3B. The buried layer 18 is formed in such a manner that it does not extend beneath the drain electrode of the second MIS field effect transistor MIS_2, that is, the portion opposing the drain electrode 10B of the MIS tetrode, or beneath the electrode 10B.

A P-type diffusion layer 28 is formed in the semiconductor substrate 30 between the surface in which the two MIS field effect transistor MIS_1 and MIS_2 are provided and the buried layer 18, and then the electrode 12 for the channel regions 3A and 3B is formed on the diffusion layer 28 in ohmic contact therewith.

With such a construction, since the buried layer 18 of high impurity concentration is formed beneath the channel regions 3A and 3B, the spreading resistance between the channel regions 3A, 3B and electrode 12 can be low and both the channel regions 3A and 3B can be connected with low resistance.

Further, since the drain region 5A of the first MIS field effect transistor MIS_1, namely the island region 33, is formed only between the channel regions 3A and 3B, the area of the P—N junction J_D at its bottom is much smaller than in the device of Figure 4, with the result that the capacity of the P—N junction J_D may be an order lower.

In the embodiment of the invention shown in Figure 5, the base region 26*b* of the transistor Tr, the first and second channel regions 3A and 3B of the MIS tetrode and the region 28 are formed by the same diffusion process, and also the emitter region 26*e* of the transistor Tr and the source regions 4A and 4B of the MIS tetrode are formed by the same diffusion process. Further, the integrated circuit shown in Figure 5 may be obtained by a similar process to that described in connection with Figures 3A to 3G.

With the embodiment of the invention described above, since the spreading resistance of the channel region of the MIS field effect transistor can be made low, its high frequency characteristics are improved. Alternative embodiments may have an N-channel.

Various modifications can be made without departing from the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. An MIS field effect transistor comprising:

a semiconductor body including:

first and second regions of semiconductor material of one conductivity type;

a third, cup-shaped, region of semiconductor material of opposite conductivity type, said third region enclosing said second region and forming a PN junction therewith and a further PN junction with said first region, and the edge of said third region being located at a surface of said body; and

a fourth region of semiconductor material of said opposite conductivity type and greater impurity concentration than said third region located beneath and in contact with said third region; and

first and second electrodes respectively connected to said first and second regions;

a gate electrode insulated from said surface and positioned over said edge of said third region; and

means to enable a potential to be applied to said third region through said fourth region.

2. A transistor according to claim 1 wherein said first region comprises a first part of higher impurity concentration in contact with said first electrode and a second part of lower impurity concentration extending from said first part to said third region.

3. A transistor according to claim 1 or claim 2 wherein said means comprises a fifth region of semiconductor material of said opposite conductivity type in contact with said fourth region, and a third electrode connected to said fifth region.

4. A transistor according to claim 1, claim 2 or claim 3, wherein said edge of said region is wholly covered by an insulating layer, and said gate electrode is positioned over a part only of said edge.

5. A transistor according to any one of the preceding claims wherein said second, third and fourth regions are diffused.

6. A transistor according to any one of the preceding claims wherein said first region is a drain, said second region is a source and said third region is a channel.

7. A transistor according to claim 6 wherein said fourth region does not extend under said drain.

8. An MIS field effect transistor substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

9. A semiconductor device substantially as described with reference to Figures 3A to 3G of the accompanying drawings.

10. A semiconductor device substantially as described with reference to Figure 5 of the accompanying drawings.

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Sheet 1

Fig. 1

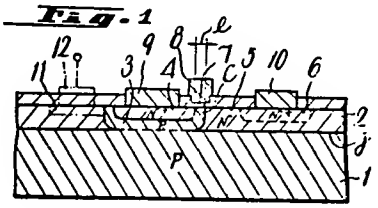

Fig. 2

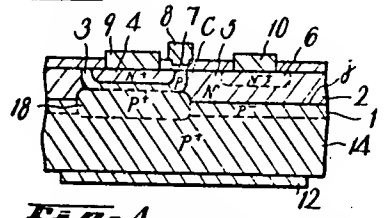

Fig. 4

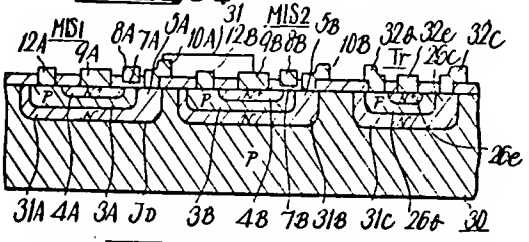

Fig. 5

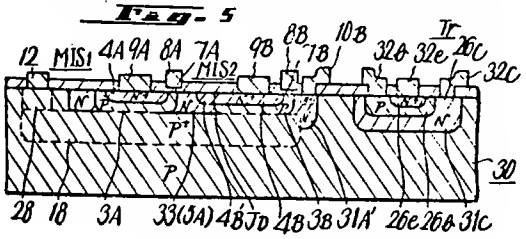

Fig. 3A

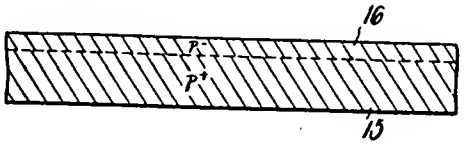

Fig. 3B

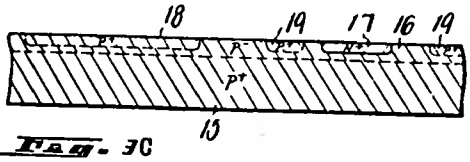

Fig. 3C

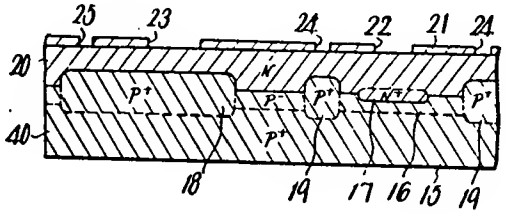

Fig. 3D

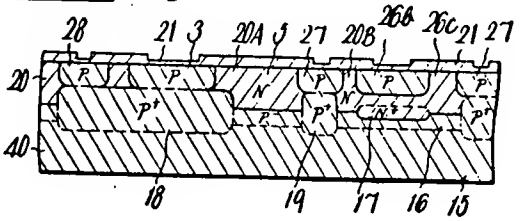

FIG. 3E

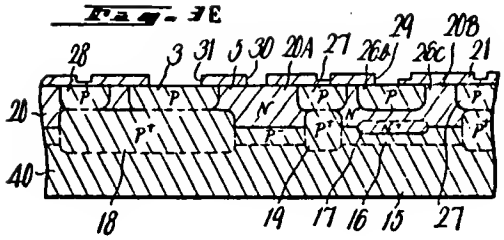

FIG. 3F

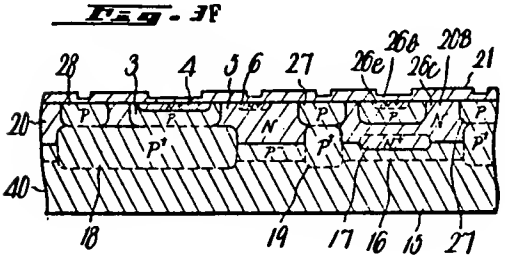

FIG. 3G